REMARKS

I. Status Summary

Claims 1-8 are pending in the present application. Claim 1 has been amended. Claims 4-8 have been canceled. Therefore, upon entry of this Amendment, Claims 1-3 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

Claims 1-3 have been amended to place the claims in better method claim format.

II. Specification

The Examiner has provided suggested guidelines for the U.S. Patent and Trademark Office's preferred layout for the specification of a utility application. In the Preliminary Amendment filed with the subject application, applicants amended the specification similar to the specification suggested by the Examiner. Applicants submit that the current layout of the specification as amended by the Preliminary Amendment satisfies the requirements of the U.S. Patent and Trademark Office.

III. Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, and 4-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the article "Computer Organization and Architecture" by William Stallings (Prentice Hall, 4th Edition, pages 9, 52, and 361-368, 1996.) (hereinafter, "Stallings"). This rejection is respectfully traversed.

Regarding Claim 1, the Examiner contended that Stallings discloses a method for branching when a program is executed by a processor and the program is stored in a program memory at Figure 3.2 on page 52. (Official Action, pages 3 and 4.) Further, the Examiner stated that Stallings discloses a variable memory and a table memory at Figure 3.2. (Stallings, page 4.) The Examiner also stated that Stallings discloses steps a-d of Claim 1 at page 364, lines 12-36, page 367, lines 28-41, and Figures 3.2 and 10.1. (Stallings, page 4.)

Upon careful consideration and review of Stallings, applicants respectfully submit that Stallings does not disclose each and every element of the presently claimed subject matter and therefore does not anticipate the presently claimed subject matter. Claim 1 has been amended to recite that steps a-d are executed by the processor within a single jump instruction. Step a has been amended to recite addressing a first memory cell in the variable memory. Step b has been amended to recite addressing a second memory cell in the variable memory on the basis of the content of the first memory cell. Step c has been amended to recite addressing a third memory cell in the table memory on the basis of the content of the second memory cell. Step d has been amended to recite execution to a program address which is stored in the third memory cell in the table memory. Summarily, Stallings does not teach a method executing steps a-d within a single jump instruction, as required by Claim 1.

Stallings teaches postindexing, autoindexing, and indirect addressing modes. (E.g., Stallings, page 367, lines 28-41.) Applicants submit that it is well known to those of ordinary skill in the relevant art that each addressing instruction must be loaded

decoded, and executed according to the Von Neuman memory configuration model. Therefore, the execution of the steps taught by Stallings are executed as independent instructions in a program code. The use of such a process for executing, for example, steps a-d recited by Claim 1 can results in high processor load and further demands for at least four memory units in the program memory because the four memory units must store the three addressing instructions and the final jump instruction.

Claim 1 requires a method for branching with a single jump instruction to execute steps a-d. This method results in reduced load on the processor and reduced memory space for storing program code as compared to the methods taught by Stallings. Additionally, the single jump instruction provides high flexibility as content of the memory cells and further parameters may be changed even after the start of the execution of the single jump instruction.

Another important benefit of this highly flexible jump instruction is that a length of the opcode for the jump instruction including the address of the first memory cell can be reduced to a minimum. For example, referring to Figure 1, the opcode of the jump instruction can contain three bits for information of the first memory cell or eight different memory cells **12** may be addressed during the jump instruction. In a conventional technique, for example, a content of the first memory cell is read out and the jump is executed to a jump destination **15** according to the content of first memory cell **12**. Thus, only eight different destinations are possible with the conventional instruction opcode. In contrast to conventional techniques, step b of Claim 1 provides a second memory cell (such as cell **13**) addressed on the basis of the content of first memory cell (such as cell **12**) and further parameters (such as parameters **11**). Thus,

in this example, the addressable state space of the second memory cell is larger than the addressable state space of the first memory cell. Therefore, the number of possible jump destinations (such as branch destination **15**) increases by the same amount. In one example, the parameters (such as parameters **11**) may be calculated before the start of the execution of the jump instruction or at the latest when the processor executes a step for reading a content of the first memory cell. Thus, the implementation of a single jump instruction according to Claim 1 can provide high flexibility in the timing of the instruction and provide high flexibility in the number of destination states (such as destination **15**). Applicants respectfully submit that a method executing steps a-d within a single jump instruction, as required by Claim 1, is entirely missing from the teachings of Stallings. For these reasons, Stallings does not teach each and every feature of Claim 1 and, thus, cannot anticipate the claim.

Claim 2 depends from Claim 1. Therefore, Claim 2 includes the features of Claim 1. Thus, the comments presented below relating to amended Claim 1 apply equally to Claim 2. For the same reasons provided for Claim 1, it is respectfully submitted that Stallings does not anticipate Claim 2.

Claims 4-8 have been canceled. Therefore, the rejection of Claims 4-8 is now moot.

For the above reasons, applicants respectfully request that the rejection of Claims 1, 2, and 4-8 under 35 U.S.C. §102(b) be withdrawn and Claims 1 and 2 allowed at this time.

IV. Claim Rejections Under 35 U.S.C. § 103

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Stallings in view of "Modern Operating Systems" by Andrew S. Tanenbaum (Prentice Hall, pages 128-130, 1992.) (hereinafter, "Tanenbaum"). This rejection is respectfully traversed.

As previously stated, Stallings fails to teach each and every element recited by Claim 1. In addition, applicants respectfully submit that Stallings fails to suggest each and every element recited by Claim 1. Tanenbaum fails to overcome the significant shortcomings of Stallings to disclose or suggest the features of amended Claim 1.

Tanenbaum teaches utilizing separate memory segments for storing different data. (Tanenbaum, page 128.) The memory segment allows its data to grow or shrink independently of other data. (Tanenbaum, page 128.) Claim 1 recites a method executing steps a-d, including addressing different memory cells, within a single jump instruction. Nowhere does Tanenbaum disclose or suggest executing steps for addressing different memory cells within a single jump instruction, as required by Claim 1. Therefore, for these reasons, Claim 1 is believed to be patentably distinguished over the combination of Stallings and Tanenbaum because the references do not disclose or suggest the presently claimed subject matter.

Claim 3 depends from Claim 1. Therefore, Claim 3 includes the features of Claim 1. Thus, the comments presented below relating to Claim 1 apply equally to Claim 3. For these reasons, Claim 3 is believed to be patentably distinguished over the combination of Stallings and Tanebaum because the references do not disclose or suggest the presently claimed subject matter.

For the above reasons, applicants respectfully submit that the teachings of Stallings and Tanenbaum, either alone or in combination, do not teach or suggest each and every feature of the present subject matter, and therefore that Claim 3 is not obvious in view of the Stallings and Tanenbaum. Applicants, therefore, respectfully request that the rejection of Claim 3 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

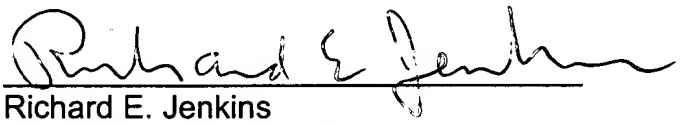
If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: December 21, 2004 By: 

Richard E. Jenkins
Registration No. 28,428
Customer No: 25297

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